circuits. Alternatively, an object is to provide a semiconductor device including a memory element. Alternatively, an object is to provide a semiconductor device that includes a memory element having a long retention period and a memory element having high operation speed. Alternatively, an object is to provide a semiconductor device that includes a plurality of kinds of memory elements and transistors whose electrical characteristics are different between the memory elements. Alternatively, an object is to provide a highly integrated semiconductor device.

Alternatively, an object is to provide a module including any of the above semiconductor devices. Alternatively, an object is to provide an electronic device including any of the above semiconductor devices or the module. Alternatively, an object is to provide a novel semiconductor device. Alternatively, an object is to provide a novel module. Alternatively, an object is to provide a novel electronic device.

Alternatively, an object is to provide a transistor having normally-off electrical characteristics. Alternatively, an object is to provide a transistor having a low leakage current in an off state. Alternatively, an object is to provide a transistor having a small subthreshold swing value. Alternatively, an object is to provide a transistor having a small short-channel effect. Alternatively, an object is to provide a transistor having excellent electrical characteristics. Alternatively, an object is to provide a transistor having high reliability. Alternatively, an object is to provide a transistor having high frequency characteristics.

Note that the descriptions of these objects do not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Other objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

(1) One embodiment of the present invention is, for example, a semiconductor device that includes a first circuit, a second circuit, and a third circuit. The first circuit includes a first transistor, a first capacitor, and a first wiring. The first transistor includes a first conductor and a first oxide semiconductor. The first conductor includes a region in contact with the first oxide semiconductor. One terminal of the first capacitor is electrically connected to the first conductor. The other terminal of the first capacitor is electrically connected to the first wiring. The second circuit includes a second transistor, a second capacitor, and a second wiring. The second transistor includes a second conductor and a second oxide semiconductor. The second conductor includes a region in contact with the second oxide semiconductor. One terminal of the second capacitor is electrically connected to the second conductor. The other terminal of the second capacitor is electrically connected to the second wiring. The third circuit includes a third transistor. The third transistor includes a third conductor, a third oxide semiconductor, a first insulator, a second insulator, and a third insulator. The third conductor includes a region in which the third conductor and the third oxide semiconductor overlap with each other. The first insulator is positioned between the third conductor and the third oxide semiconductor. The second insulator is positioned between the third conductor and the first insulator. The third insulator is positioned between the third conductor and the second insulator. The second insulator includes an electron trap region. A gate voltage at which a drain current in a subthreshold region is 1×10^{-12} A is greater than or equal to 0.8 V and less than or equal to 1.5 V in the first transistor. A gate voltage at which a drain current in a subthreshold region is 1×10^{-12} A is greater than or equal to 0 V and less than or equal to 0.7 V in the second transistor.

(2) Alternatively, one embodiment of the present invention is the semiconductor device described in (1), in which the second insulator is an oxide or a nitride containing boron, aluminum, silicon, scandium, titanium, gallium, yttrium, zirconium, indium, lanthanum, cerium, neodymium, hafnium, or thallium.

(3) Alternatively, one embodiment of the present invention is the semiconductor device described in (1) or (2), in which the first transistor further includes a fourth conductor, a fourth insulator, a fifth insulator, and a sixth insulator; the fourth conductor includes a region in which the fourth conductor and the first oxide semiconductor overlap with each other; the fourth insulator is positioned between the fourth conductor and the first oxide semiconductor; the fifth insulator is positioned between the fourth conductor and the fourth insulator; the sixth insulator is positioned between the fourth conductor and the fifth insulator; and the fifth insulator includes a negatively charged region.

(4) Alternatively, one embodiment of the present invention is the semiconductor device described in (3), in which the fifth insulator is an oxide or a nitride containing boron, aluminum, silicon, scandium, titanium, gallium, yttrium, zirconium, indium, lanthanum, cerium, neodymium, hafnium, or thallium.

(5) Alternatively, one embodiment of the present invention is the semiconductor device described in any one of (1) to (4), in which the second transistor further includes a fifth conductor, a seventh insulator, an eighth insulator, and a ninth insulator; the fifth conductor includes a region in which the fifth conductor and the second oxide semiconductor overlap with each other; the seventh insulator is positioned between the fifth conductor and the second oxide semiconductor; the eighth insulator is positioned between the fifth conductor and the seventh insulator; the ninth insulator is positioned between the fifth conductor and the eighth insulator; and the eighth insulator includes a negatively charged region.

(6) Alternatively, one embodiment of the present invention is the semiconductor device described in (5), in which the eighth insulator is an oxide or a nitride containing boron, aluminum, silicon, scandium, titanium, gallium, yttrium, zirconium, indium, lanthanum, cerium, neodymium, hafnium, or thallium.

(7) Alternatively, one embodiment of the present invention is the semiconductor device described in any one of (1) to (6), in which the first transistor further includes a sixth conductor and a ninth insulator; the sixth conductor includes a region in which the sixth conductor and the first oxide semiconductor overlap with each other; and the ninth insulator is positioned between the sixth conductor and the first oxide semiconductor.

(8) Alternatively, one embodiment of the present invention is the semiconductor device described in (7), in which the first transistor further includes a tenth insulator and an eleventh insulator; the tenth insulator is positioned between the sixth conductor and the ninth insulator; the eleventh insulator is positioned between the sixth conductor and the tenth insulator; and the tenth insulator includes a negatively charged region.

(9) Alternatively, one embodiment of the present invention is the semiconductor device described in (8), in which the tenth insulator is an oxide or a nitride containing boron,